
REMARKS**Drawings**

The drawings were objected to as failing to comply with 37 CFR 1.84(l), (m) and (t). Applicant has enclosed formal drawings to address this rejection.

The drawings were also objected to under 37 CFR 1.83(a), as the drawings must show every feature of the invention specified in the claims.

The Applicant disagrees with the Examiner and believes that no further drawings are required under 37 CFR 1.83(a). The Examiner stated that “[t]he drawings must show every feature specified in the claims. Therefore the method must be shown or the feature(s) canceled from the claim(s).” (Office Action mailed March 30, 2004, Page 2) The Applicant respectfully submits that drawings are not required for method claims for, as stated in MPEP §601.01(f), “[i]t has been USPTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 U.S.C. 113 (first sentence).”

The Applicant therefore requests removal of the objections to the drawings by the Examiner under 37 CFR 1.84(l), (m) and (t) and under 37 CFR 1.83(a). The Applicant also requests approval of the formal drawings.

Claim Objections

Claims 16-33 and 38-41 were objected to due to the following alleged informalities: 37 C.F.R. 1.83(a) states the drawings must show every feature of the invention specified in the claims. As stated above, MPEP §601.01(f) indicates that no further drawings are required.

Rejections Under 35 U.S.C. § 112, first paragraph

Claims 34-41 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Applicant traverses the rejection and believes that claims 34-41 are allowable for the following reasons.

The Examiner stated that claims 34-41 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner stated that “[i]ndependent claims 34, 38 and 41 recite variables, which are not defined.” (Office Action mailed March 30, 2004, Page 3)

The Applicant maintains that X and Y represent nominal values of data bits and data connections and that the claims are defined by the relationship of X and Y as detailed in the specific claim. Applicant contends that each use of X or Y in a claim signifies the same value as is apparent in the context of the claim and Applicant’s Specification. *See e.g.*, MPEP §2163.02; the Applicant also notes MPEP §2163.03, which states that “rejection of an original claim for lack of written description should be rare.”

Applicant therefore respectfully requests that the rejection of the claims 34-41 under 35 U.S.C. § 112, first paragraph, be withdrawn in light of the above arguments and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 28-33 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Applicant traverses this rejection and feels that claims 28-33 are allowable for the following reasons.

The Examiner rejected independent claim 28 as indefinite, stating that “the term ‘X’ is not defined in the claim, such as ‘where x is a positive integer greater than 1.’” (Office Action mailed March 20, 2004, Page 4) The Applicant notes that, as defined by MPEP §2173, “[t]he primary purpose of this requirement of definiteness of claim language is to ensure that the scope of the claims is clear so the public is informed of the boundaries of what constitutes infringement of the patent.” Applicant contends that the scope of the claims is definite to one skilled in the art.

With respect to claim 28, Applicant maintains that the term “X” of claim 28, a “method of testing a memory device having X selectable tests,” refers to a number of possible tests that the memory device can perform. This number is inherently an integer

value and thus is sufficiently defined to render the claim definite. *See, e.g.*, MPEP § 2173 and § 2173.02. As claims 29-33 depend from and further define claim 28 and they are also considered to be allowable. The Applicant therefore respectfully requests that the rejection of claims 28-33 under 35 U.S.C. § 112, second paragraph to be withdrawn.

The Examiner rejected claims 20, 22-23, 27, 32-33 and 38-39 as indefinite, stating that the phrase “prohibiting the test mode” contained in claims 20, 22-23, 27, 32-33 and 38-39 is unclear. The Examiner further stated that “[f]or purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode.” (Office Action mailed March 20, 2004, Pages 5-6)

Applicant acknowledges that the Examiner’s assumption is correct and that “prohibiting the test mode” refers to preventing the memory device from entering the test mode of operation. Applicant refers to the paragraph starting on line 15, page 11 of the Specification, which states in part, “[a] test mode must be entered to initiate a test operation on the memory device. During production testing, a software command can be used to enter the test mode. That is, providing a specific command sequence to the memory can enter the test mode. To prevent a user from accidentally initiating a test mode operation, a non-volatile data register 180 is provided.” Applicant therefore submits that the expression “prohibiting the test mode” presents no uncertainty or ambiguity with respect to the question of scope or clarity of the claim and is also the claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art and that claims 20, 22-23, 27, 32-33 and 38-39 are allowable. Applicant therefore respectfully requests that the rejection of claims 20, 22-23, 27, 32-33 and 38-39 under 35 U.S.C. § 112, second paragraph to be withdrawn.

With respect to claims 21, 24 and 40, Applicant respectfully submits that the phrase “a high voltage signal is detected on a pre-determined address input” refers to the memory device detecting an elevated voltage from that of a normal signal level on a selected address input. Applicant refers to the paragraph starting on line 15, page 11 of the Specification, which further states in part, “[f]or example, an elevated voltage must be provided on a pre-selected address input connection to initiate a test mode. Thus, a

voltage detection circuit 190 monitors the address input. Once an elevated voltage is detected, the test mode is entered and a selected test can be specified.” The Applicant therefore submits that the expression “a high voltage signal is detected on a pre-determined address input” presents no uncertainty or ambiguity with respect to the question of scope or clarity of the claim and is also a claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art and that claims 21, 24 and 40 are allowable. The Applicant therefore respectfully requests that the rejection of claims 21, 24 and 40 under 35 U.S.C. § 112, second paragraph be withdrawn.

With respect to claims 27 and 41, Applicant respectfully submits that, as discussed above with claims 21, 24 and 40 and claims 20, 22-23, 27, 32-33 and 38-39, the phrase “prohibiting the test mode” refers to preventing the memory device from entering the test mode of operation and the phrase “a high voltage signal is detected on a pre-determined address input” refers to the memory device detecting an elevated voltage from that of a normal signal level on a selected address input. The Applicant therefore submits that both phrases are clearly defined.

The Applicant also respectfully submits that, in further respect to claim 27, the phrase of line 9, “selecting a test mode in response to a test code provided on the address inputs,” is not unclear and has antecedent basis in the phrase “receiving test mode commands on address inputs” of line 3 of claim 27. This clearly differentiates it over “a pre-determined address input” noted by the Examiner in the claim term starting on line 6, which states “placing the non-volatile memory device in the test mode if the test latch circuit is in the second state, and a high voltage signal is detected on a pre-determined address input.”

The Applicant therefore submits that claims 27 and 41 present no uncertainty or ambiguity with respect to the question of scope or clarity of the claims. The Applicant thus submits that claims 27 and 41 are allowable. The Applicant therefore respectfully requests that the rejection of claims 27 and 41 under 35 U.S.C. § 112, second paragraph to be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1-5, 7-12 and 14-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Roohparvar (U.S. Patent 5,526,364). Applicant respectfully traverses this rejection and feels that claims 1-5, 7-12 and 14-27 are allowable for the following reasons.

Applicant respectfully maintains that Roohparvar teaches a memory which receives a test code on the I/O (bi-directional data) lines to select the test mode and enters the test mode upon receiving a high voltage on two terminals. *See, e.g.*, Roohparvar, Abstract, Figure 1, and column 2, line 54 to column 3, line 3, and column 3, lines 7-43. Applicant therefore respectfully maintains that Roohparvar does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. Applicant contends that address inputs do not correspond to Roohparvar's I/O lines.

Applicant's claim 1 recites, in part, "address input connections to receive externally provided signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the externally provided signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose such a non-volatile memory device that initiates a test mode selected by test codes received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 1.

Applicant's claim 7 recites, in part, "address input connections to receive externally provided address and test mode code signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose such a flash memory device that initiates a test mode selected by test codes received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 7.

Applicant's claim 16 recites, in part, "selecting a test mode in response to a test code provided on address inputs." As detailed above, Applicant submits that Roohparvar fails to teach or disclose such a method that selects a test mode in response to test codes

received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 16.

In regards to claims 14-15, the Applicant notes that Applicant's claim 13 recites, in part, "address input connections to receive externally provided address and test mode code signals from the external memory controller" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose placing a memory device in a test mode selected by test codes received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 13. As claims 14-15 depend from and further define claim 13, they are also considered to be in condition for allowance.

In regards to claims 22-27, the Applicant notes that Applicant's claim 22 recites, in part, "selecting a test mode in response to a test code provided on the address inputs." As detailed above, Applicant submits that Roohparvar fails to teach or disclose selecting a test mode in response to a test code provided on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 22.

Applicant's claim 25 recites, in part, "receiving a test code command on address input connections" and " wherein the test code command instructs the memory device to perform a selected test operation." As detailed above, Applicant submits that Roohparvar fails to teach or disclose receiving a test code command on address input connections and wherein the test code command instructs the memory device to perform a selected test operation. As such, Roohparvar fails to teach or disclose all elements of independent claim 25.

Applicant's claim 27 recites, in part, "selecting a test mode in response to a test code provided on the address inputs." As detailed above, Applicant submits that Roohparvar fails to teach or disclose selecting a test mode in response to a test code provided on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 27.

Applicant respectfully contends that claims 1, 7, 13, 16, 22, 25 and 27 have been shown to be patentably distinct from the cited reference. As claims 2-5, 8-12, 14-21, 23-24 and 26 depend from and further define claims 1, 7, 13, 16, 22 and 25, respectively,

they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1-5, 7-12 and 14-27.

Claims 1-3, 7-9, 16 and 17 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Akaogi et al. (U.S. Patent 6,550,028). Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant feels that claims 1-3, 7-9, 16 and 17 are allowable for the following reasons.

Applicant respectfully maintains that Akaogi et al. teaches a non-volatile memory which allows the threshold voltage distribution of its floating gate memory array to be tested. The non-volatile memory device of Akaogi et al. does this by entering a test mode upon receiving specified combination on the chip enable 202, output enable 204, write enable 206, accelerate input 208, and reset input 210. An analog test voltage can then be directly applied through the ready/busy input 212 to the floating gate transistors selected by the address applied to the address inputs 102 to test their threshold voltage levels. Results of the threshold voltage test (the transistors that have been programmed at the applied test voltage) are read from the data output 192 in 8 or 16 bit result modes, dependent on a BYTE input pin that selects byte or word output in normal or test mode of operation. *See, e.g.,* Akaogi et al., Figures 1 and 2, column 14, lines 31-62, and column 12, line 30 to column 13, line 50. Applicant therefore respectfully maintains that Akaogi et al. does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. Applicant contends that address inputs do not correspond to Akaogi et al.'s specified combination on the chip enable, output enable, write enable, accelerate input and reset input lines.

Applicant's claim 1 recites, in part, "address input connections to receive externally provided signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the externally provided signals." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a non-volatile memory device that initiates a test mode

selected by test codes received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 1.

Applicant's claim 7 recites, in part, "address input connections to receive externally provided address and test mode code signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a flash memory device that initiates a test mode selected by test codes received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 7.

Applicant's claim 16 recites, in part, "selecting a test mode in response to a test code provided on address inputs." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a method that initiates a test mode selected by test codes received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 16.

Applicant respectfully contends that claims 1, 7 and 16 have been shown to be patentably distinct from the cited reference. As claims 2-3, 8-9 and 17 depend from and further define claims 1, 7 and 16, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1-3, 7-9, 16 and 17.

Claims 28 and 29 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Fang et al. (U.S. Patent 5,802,071). Applicant respectfully traverses this rejection and feels that claims 28 and 29 are allowable for the following reasons.

Applicant respectfully maintains that Fang et al. teaches a micro-controller and test machine that can execute a test of the micro-controller from an external test circuit, a built-in test circuit, and an test application to provide a flexible test pattern. *See, e.g.*, Fang et al., Abstract, Figures 3 and 4, column 2, line 60 to column 3, line 58. Applicant therefore respectfully maintains that Fang et al. does not teach or disclose a method of testing a memory device, but a method of testing a micro-controller. The Applicant further maintains that Fang et al. does not teach or disclose a memory device that initiates

a test mode selected by test codes received on the address inputs, but a micro-controller that selects test modes and reads test executables through separate data “channels”.

Applicant contends that memory device address input connections do not correspond to Fang et al.’s channels.

Applicant’s claim 28 states, in part, “a method of testing a memory device”, and “selecting one of the X selectable tests using a test code provided on address input connections.” As detailed above, Applicant submits that Fang et al. fails to teach or disclose such a memory device that initiates a test mode selected by test codes received on the address inputs. As such, Fang et al. fails to teach or disclose all elements of independent claim 28.

Applicant respectfully contends that claim 28 has been shown to be patentably distinct from the cited reference. As claim 29 depends from and further defines claim 28 it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 28 and 29.

Rejections Under 35 U.S.C. § 103

Claims 4-6, 10-12, 13-15 and 18-19 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Akaogi et al. (U.S. Patent 6,550,028) in view of Sher et al. (U.S. Patent 6,154,851). Applicant respectfully traverses this rejection and feels that claims 4-6, 10-12, 13-15 and 18-19 are allowable for the following reasons.

Applicant contends that it has shown claims 1, 7 and 16 to be patentably distinct from the Akaogi et al. reference. The secondary reference of Sher et al. fails to overcome the deficiencies of the Akaogi et al. reference. Thus, claims 1, 7 and 16 are patentably distinct from the cited references, either alone or in combination. As claims 4-6, 10-12 and 18-19 depend from and further define one of claims 1, 7 or 16, these claims are also believed to be allowable.

In regards to independent claim 13, the Applicant respectfully submits that, as stated above, Akaogi et al. fails to teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. As such, Akaogi et al. fails

to teach or suggest all elements of independent claim 13. In addition, Sher et al. also does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. Therefore combining the elements of Akaogi et al. with Sher et al. does not teach or suggest all elements of claim 13. The Applicant therefore maintains that claim 13 is thus allowable over Akaogi et al. and Sher et al., either alone or in combination. As claims 14-15 depend from and further define claim 13, claims 14-15 are also deemed allowable.

Applicant respectfully contends that claims 4-6, 10-12, 13-15 and 18-19 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 4-6, 10-12, 13-15 and 18-19.

CONCLUSION

Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact the under-signed directly at (612) 312-2207.

Respectfully submitted,

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Andrew C. Walseth
Reg. No. 43,234

Attorneys for Applicant
Leffert Jay & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009
Phone: (612) 312-2200
Fax: (612) 312-2250